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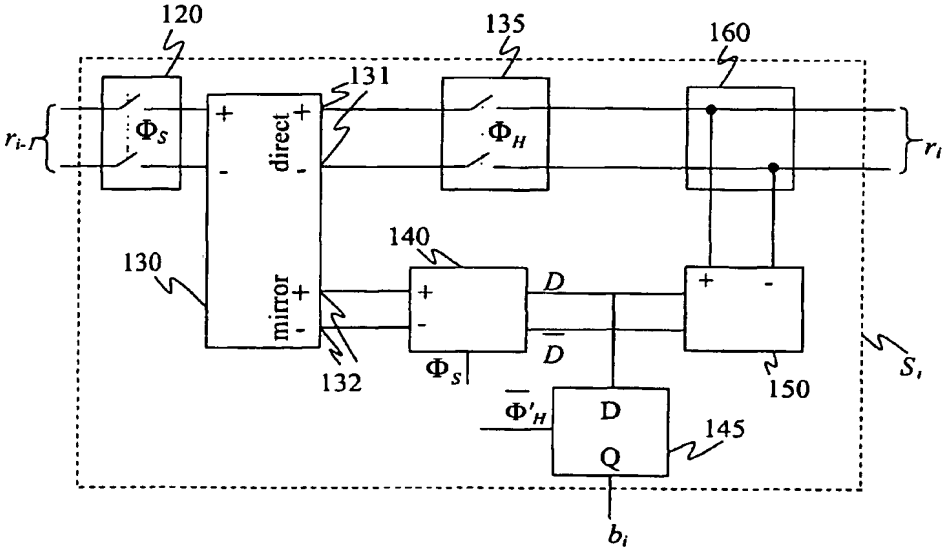
(54) Title: SWITCHED-CURRENT ANALOGUE-TO-DIGITAL CONVERTER



(57) Abstract: A current mode analogue-to-digital converter uses a conversion stage which operates using a two-phase clock and which requires the input signal to be present during only one of the phases. A sample-and-hold circuit (120, 130, 135) samples the input signal during the first clock phase and during the second clock phase a quantised bit value is generated from a mirror of the held input current by a kickback-free comparator circuit (140). Also during the second clock phase a residue is generated using the quantised value and a non-mirrored version of the held input current. Optionally, two comparator circuits (140, 140") may be used to provide two-level quantisation, enabling errors introduced by the current mirror to be corrected by a Redundant Signed Digit algorithm. Two pipelines of conversion stages ($S_{i'}$, $S_{i''}$) can be multiplexed to double the conversion rate.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M1/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 313 780 B1 (HUGHES JOHN B ET AL) 6 November 2001 (2001-11-06) ---	
A	SROWIK R ET AL: "Low-power class AB current memory cell" , ELECTRONICS LETTERS, IEE STEVENAGE, GB, VOL. 35, NR. 23, PAGE(S) 2014-2015 XP006012931 ISSN: 0013-5194 --- -/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 February 2004	16/02/2004

Name and mailing address of the ISA	Authorized officer
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Internal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	BRACEY M ET AL: "A 70MS/S 8-BIT DIFFERENTIAL SWITCHED-CURRENT CMOS A/D CONVERTER USING PARALLEL INTERLEAVED PIPELINES" , 1995 IEEE TENCON. IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI. HONG KONG, NOV. 6 - 10, 1995, IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI.(TENCON), NEW YORK, IEEE, US, PAGE(S) 143-146 XP000585762 ISBN: 0-7803-2625-3	

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US 6313780 B1	06-11-2001	WO 0019614 A2	06-04-2000
		EP 1046231 A2	25-10-2000
		JP 2002526964 T	20-08-2002